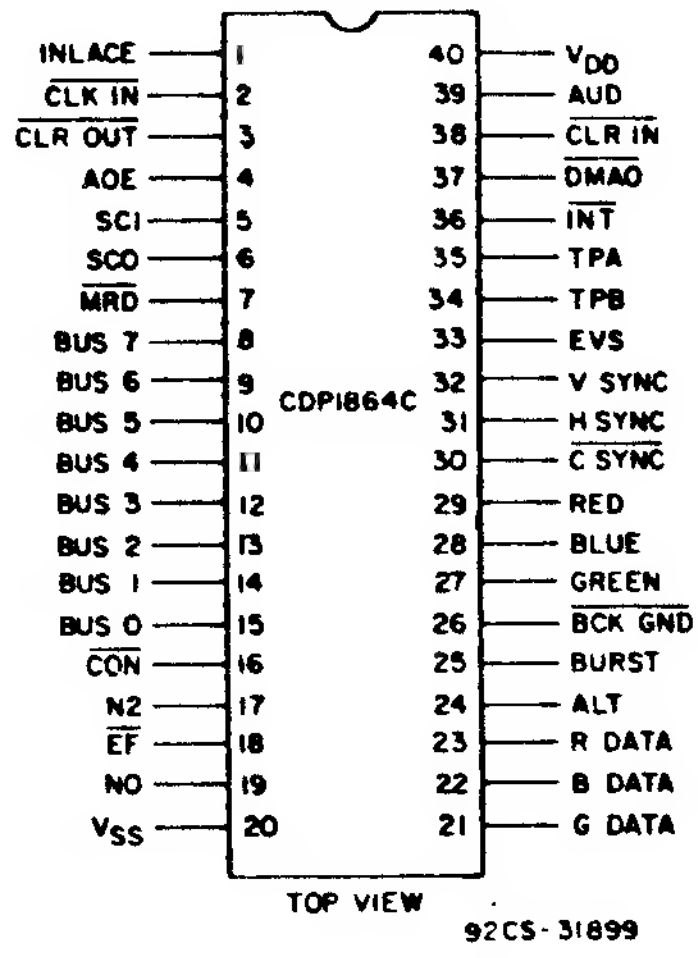
CDP1864C Types

COS/MOS PAL Compatible Color TV Interface

Objective Data

Features:

- Single chip contains circuitry for video, sync, RGB color, and programmable frequency for tone generation
- Programmable 1-of-8 dot colors plus 1-of-4 background colors
- Bit-mapped display with maximum resolution of 192 vertical x 64 horizontal
- Directly interfaces with CDP1800 series microprocessors
- Interlaced or non-interlaced displays
- Schmitt trigger clear input and output for power-on reset of CDP1800 system
- 1.75-MHz crystal operation
- Single 4.75 to 6.5 V supply
- Low-power static CMOS circuitry
- High noise immunity



TERMINAL ASSIGNMENT

The RCA-CDP1864C is an LSI CMOS color or black and white PAL-compatible video controller designed for use in CDP1800 microprocessor systems. It interfaces directly with the CDP1802 and CDP1804 as shown in Figs. 1 and 2. The DMA feature of these processors is used for direct data transfers of luminance information for display refresh. The INTERRUPT input and a flag line (EF1, EF2, EF3, or EF4) are used for handshaking.

The CDP1864C generates vertical sync, horizontal sync, and composite sync. These signals, combined with the RED, BLUE, GREEN, BURST, and BACKGROUND signals, can be used to generate a composite video signal, or they can be used directly inside a TV set.

In addition to generating a bit-mapped video display the CDP1864C contains a programmable frequency generator designed to produce 256 tones that range from 107 Hz to 13672 Hz.

The CDP1864C is supplied in the 40-lead dual-in-line ceramic (D suffix) and plastic (E suffix) packages.

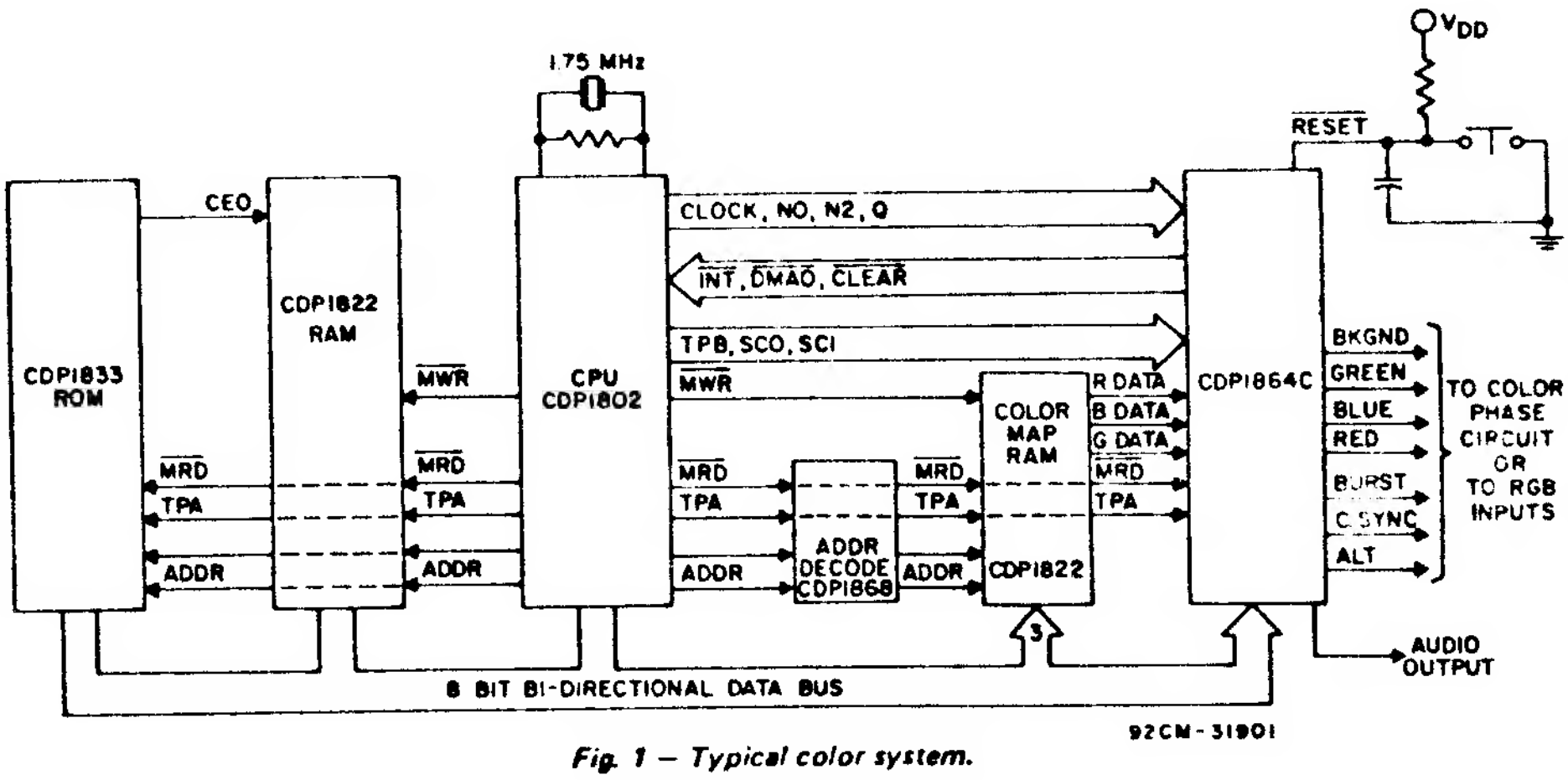


Fig. 1 — Typical color system.

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MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltage referenced to V_{SS} Terminal)
CDP1864C . . . . . −0.5 to +7 V
INPUT VOLTAGE RANGE, ALL INPUTS . . . . . −0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT . . . . . ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = −40 to +60°C (PACKAGE TYPE E) . . . . . 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) . . . . . Derate Linearly at 12 mW/°C to 200 mW
For T_A = −55 to +100°C (PACKAGE TYPE D) . . . . . 500 mW
For T_A = +100 to +125°C (PACKAGE TYPE D) . . . . Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) . . . . . 100 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, H . . . . . −55 to +125°C
PACKAGE TYPE E . . . . . −40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg}) . . . . . −65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . . +265°C

OPERATING CONDITIONS at T_A = Full Package Temperature Range

For maximum reliability, operating conditions should be selected to that operation is always within the following ranges:

CHARACTERISTIC	V_{DD} (V)	TYPICAL VALUES	UNITS
DC Operating-Voltage Range	–	4 to 6	V
Input Voltage Range	–	V_{SS} to V_{DD}	V
Maximum Input Pulse Rise or Fall Time, t_r,t_f	5	5	μs
Maximum Input Clock Frequency, f_{CL}	5	2	MHz

STATIC ELECTRICAL CHARACTERISTICS at T_A = 25°C, V_{DD} = 5 V ±5%

CHARACTERISTIC	TEST CONDITIONS		LIMITS			UNITS
			CDP1864C			
	V_O (V)	V_{IN} (V)	Min.	Typ.	Max.	
Quiescent Device Current, I_{DD}	–	0,5	–	100	500	μA
Output Voltage:*						
Low-Level, V_{OL}	–	0,5	–	0	0.05	V
High-Level, V_{OH}	–	0,5	4.95	5	–	V
Input Low Voltage, V_{IL}	0.5,4.5	Any Input	–	–	1.5	V
Input High Voltage, V_{IH}	0.5,4.5	Any Input	–	–	3.5	V
Output Low (Sink) Current, I_{OL}	0.4	0,5	2	2.4	–	mA
Output High (Source) Current, I_{OH}	4.5	0,5	−1.6	−1.8	–	mA
Input Leakage Current, I_{IL},I_{IH}	–	Any Input	–	±0.1	±1	μA
3-State Output Leakage Current, I_{OUT}	0.5	0,5	–	±0.2	±2	μA

*$I_O \leq 1$ μA.

CDP1864C Types

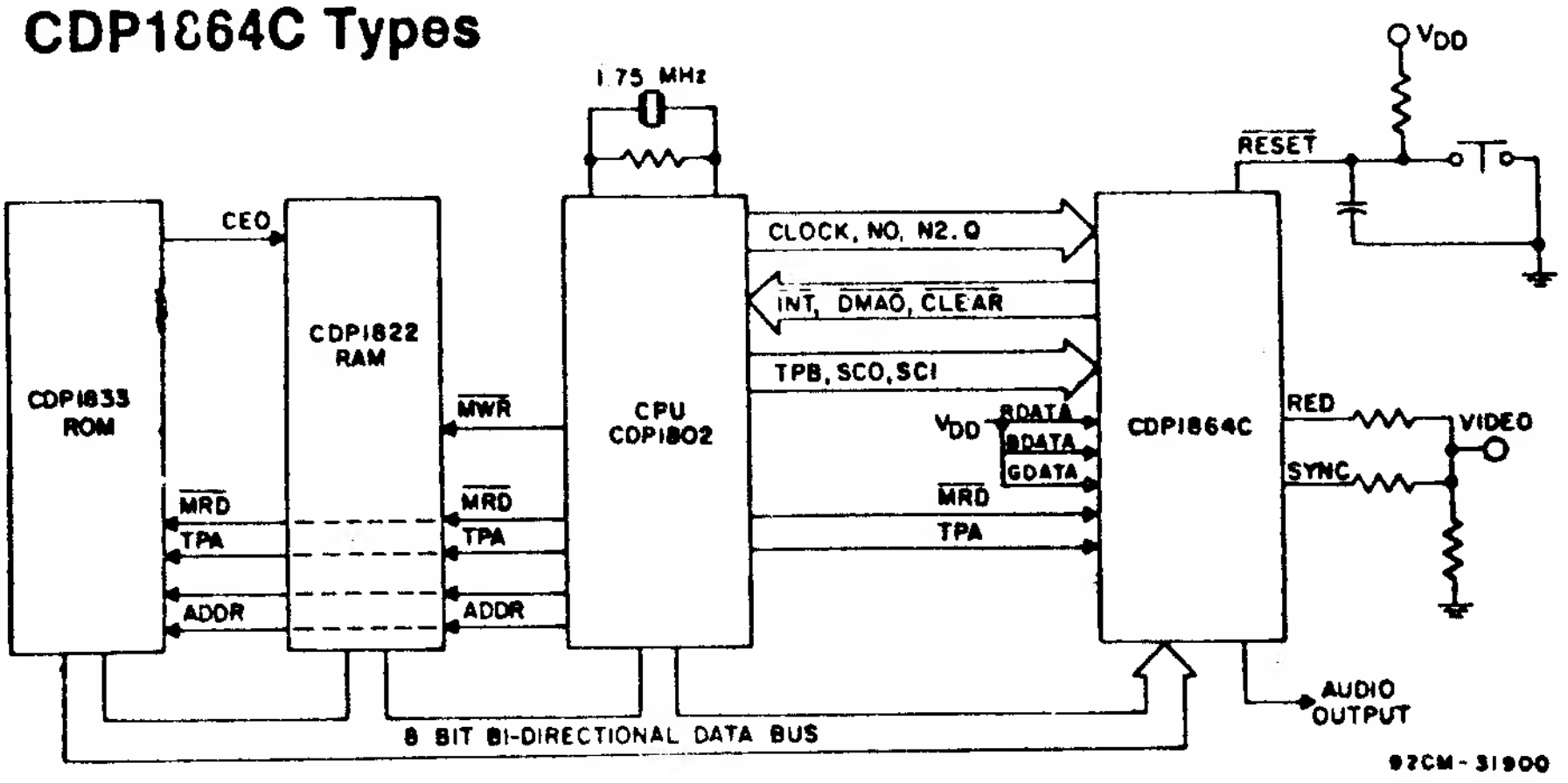

Fig. 2 – Typical black and white system.

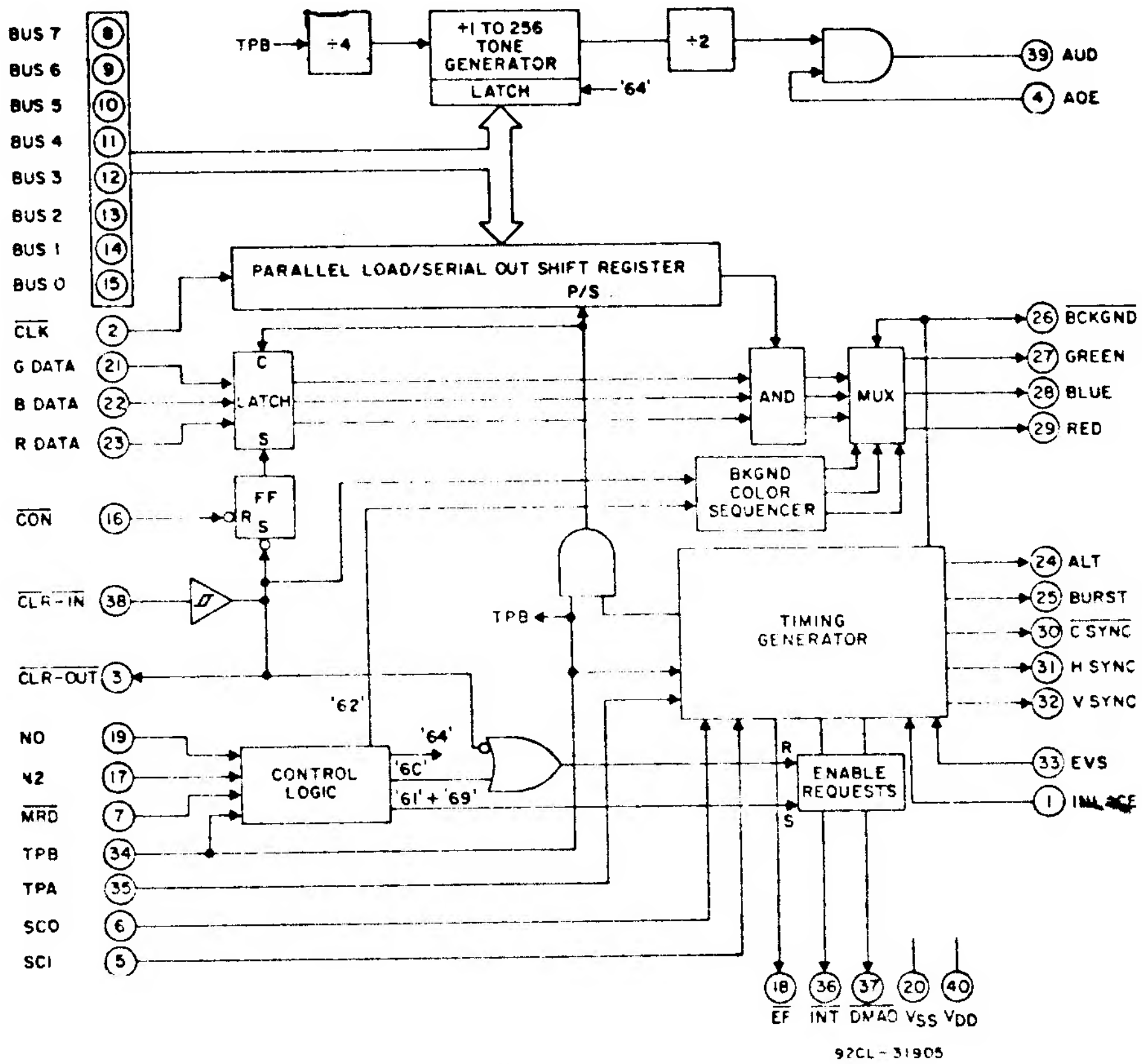

Fig. 3 – CDP1864C block diagram.

CDP1864C Types

CIRCUIT OPERATION

The CDP1864C consists of four major sections: a timing generator that produces the necessary signals for video interface, a parallel-in/serial out shift register for dot generation, a tone generator for one of 256 frequencies, and control logic for software control of the first three sections (see Fig. 3). In a typical CDP1800 system, control of the CDP1864C is accomplished with I/O commands as shown in Fig. 5.

The CDP1864C display is a bit-mapped, color or black and white display with a maximum resolution of 192 lines vertically and 64 dots (eight 8-bit bytes) horizontally. This resolution, which requires 1.5 kbytes of refresh RAM, is seldom used because of the poor aspect ratio of the resultant picture element. An approximately square picture element is obtained by repeating each horizontal line 6 times (this is done in software by the CPU) for a 32-row by 64-dot display. This lower resolution display requires 256 bytes of refresh RAM.

The CDP1864C generates both composite and separate horizontal and vertical sync, RED, BLUE, GREEN, BURST, and BACKGROUND signals. These signals may be used directly (inside the TV), or they may be used to generate the composite video signal. The sync signals generate either a 625 line-per-frame interlaced display or a 312 line-per-frame non-interlaced display. This is selectable by connecting the INTERLACE input to either V_{DD} or GND.

The video refresh is accomplished via the DMA channel of the microprocessor, and synchronization is provided by $\overline{INT}$, $\overline{EF}$, SC0, and SC1. The $\overline{EF}$ signal goes low 4 horizontal lines prior to the start of display and again 4 lines prior to the end of the display. This signal alone can be used by the CPU to initialize R(0) for DMA refresh. Alternatively, the $\overline{INT}$, which goes low 2 lines prior to the start of the display, may be used to enter an interrupt routine that initializes R(0), and the $\overline{EF}$ signal can be used to indicate the end of the display. The combination of $\overline{INT}$ and $\overline{EF}$ allows for an interrupt routine to oversee DMA refresh and repeat horizontal lines for configurations with less than the maximum 192-line resolution. $\overline{EF}$ can be sampled to detect the end of the display and cause a return to the main program from the interrupt routine.

SC1 and SC0 are used to provide CDP1864C-to-CPU synchronization for a jitter-free display. During every horizontal sync the CDP1864C samples SC0 and SC1 for SC0 = 1 and SC1 = 0 (CDP1800 execute state). Detection of a fetch cycle causes the CDP1864C to skip cycles to attain synchronization. Once in lock the system will remain locked if: (1) no 3-cycle instructions (e.g. NOP) are executed during the display (three 2-cycle instructions are executed each horizontal line); (2) an even number of cycles is performed between frames (easiest to do by avoiding 3-cycle instructions); or (3) exactly 29 cycles, beginning with a fetch and ending with an execute, are completed between the S3 interrupt response of the cpu and the first DMA in systems using $\overline{INT}$. The 29 cycles of interrupt should consist of an early 3-cycle instruction and thirteen 2-cycle instructions (or equivalent). Fig. 5 is an example of an interrupt routine for a 64 by 32 picture element display (each horizontal line is repeated 6 times).

Reset disables the color, control, $\overline{INT}$, and $\overline{DMA}$ requests. A 61 or 69 instruction enables the requests, and a 6C instruction disables them (see Fig. 5). Color is enabled by $\overline{CON}$, which is normally connected to the gated $\overline{MWR}$ signal of the color RAM.

The background color is program-selected to be either blue, black, green, or red. The initial default is blue. The color selected is changed by a 61 instruction (see Fig. 5). This condition causes the color to step to the next color in the order shown above. From red it steps to blue. The BACKGROUND output may be used to lower the luminance of the color when it is background. This would, for instance, enable a blue spot to be used on a blue background and still be visible. The BACKGROUND signal and RGB outputs are internally blanked during the horizontal and vertical retrace.

The CDP1864C also contains a programmable tone generator designed to produce 256 frequencies. The frequency input to this generator is the TPB input (TPB frequency = 1.75 MHz ÷ 8 = 218.75 kHz). This frequency is further reduced by a divide-by-4 predivider, an 8-bit programmable up-counter, and a divide-by-2 output stage. The programmable up-counter is reloaded automatically from the 8-bit tone generator latch each time it reaches the terminal count. The tone generator latch is loaded by the CPU from the data bus during a 64 output instruction (see Fig. 5).

An AUDIO OUTPUT ENABLE (AOE) terminal is also provided. When this terminal is high the output of the generator (AUDIO OUT) is allowed to toggle freely. When this terminal is low the output is held low. AUDIO OUT may be connected to the Q line of the CDP1802/CDP1804. A low on the reset sets the 8-bit latch to a default state of 35 hex and resets the programmable counter. When reset is released a frequency output of 506 will be generated until a new value is loaded into the latch. The frequencies generated from the input to the 8-bit tone generator latch can be computed by:

$$f = \frac{27343.75}{(\text{Hex Code} + 1)_{10}} \text{ Hz.}$$

CDP1864C Types

FUNCTIONAL DESCRIPTION OF CDP1864C TERMINALS

INLACE – INTERLACE (Input):
A high level at this input results in the generation of a 625 line-per-frame interlaced display, and a low-level input results in the generation of a 312 line-per-frame non-interlaced display.

$\overline{\text{CLK IN}}$ – $\overline{\text{CLOCK INPUT}}$ (Input):
A 1.75 MHz clock input to the XTAL terminal of the CDP1802/CDP1804.

$\overline{\text{CLR OUT}}$ – $\overline{\text{CLEAR OUT}}$ (Output):
This is a post-Schmitt trigger output of the signal on CLR IN. It is connected to the CLEAR-N input of the CDP1802 to provide it with a clean, clear signal.

AOE – AUDIO OUTPUT ENABLE (Input):
A high level at this input allows the selected frequency to be generated at the AUDIO-OUT terminal. A low-level input holds AUDIO OUT low. AOE may be connected to Q output of the CDP1802/CDP1804.

SC0, SC1 – STATE CODES 0 AND 1 (Inputs):
These inputs are used to synchronize the CDP1864 to the microprocessor machine states and are connected to the SC1 and SC0 outputs of the CDP1802/CDP1804.

$\overline{\text{MRD}}$ – (Input):
This input selects the command issued to the CDP1864 (in conjunction with N2 and NO). It is connected to the MRD output of the CDP1802/CDP1804.

BUS 0 – BUS 7 (Inputs):
These inputs load the luminance information during the display interval, and the frequency generator divide byte when selected. They are connected to the DATA BUS.

$\overline{\text{CON}}$ – $\overline{\text{COLOR ON}}$ (Input):
A low level at this input enables the CDP1864 to begin loading color information form the RDATA, GDATA, and BDATA inputs. CON is connected to the gated MWR signal of the color memory.

N2 (Input):
This input is used in conjunction with $\overline{\text{MRD}}$ and TPB to load data into the tone generator latch (MRD·N2·TPB) and disable the generation of INTERRUPT and DMA requests by the CDP1864 ($\overline{\text{MRD}}$·N2·TPB). For example, a 64 instruction would result in data being loaded into the tone-divider latch, while a 6C instruction would disable the INTERRUPT and DMA requests. N2 is connected to the N2 output of the CDP1802/CDP1804.

$\overline{\text{EF}}$ – $\overline{\text{EXTERNAL FLAG OUT}}$ (Output):
This output is connected to a CDP1802/CDP1804 $\overline{\text{EXTERNAL FLAG}}$ input. It maintains software synchronization with the display. Two pulses per field are generated on this line, each of which is four horizontal lines wide. The first pulse begins four horizontal lines before the display, and the second pulse begins four horizontal lines prior to the end of the display. The second pulse is used to indicate to the microprocessor that the display is ending.

NO (Input):
This input is used in conjunction with $\overline{\text{MRD}}$ and TPB to step the background color (MRD·NO·TPB) and to enable the INTERRUPT and DMA requests (NO·TPB). For example, a 61 instruction would step the background color, and a 61 or 69 instruction would enable the INTERRUPT and DMA requests. NO is connected to the NO output of the CDP1802/CDP1804.

V_{SS}:
Negative supply voltage.

GDATA, BDATA, RDATA – RED, GREEN, and BLUE DATA (Inputs):
These inputs carry color information from the color RAM. The data on these lines are latched concurrent with the latching of the luminance information from the data bus during the display interval if the $\overline{\text{CON}}$ input has gone low since reset.

ALT – ALTERNATE (Output):
This output toggles at each horizontal sync time and is used to perform the phase alternation.

BURST (Output):
This output applies a 4.57 us pulse to each horizontal sync back-porch (except for 24 lines during vertical sync when it is blanked) which gates in the color burst signal.

$\overline{\text{BCKGND}}$ – $\overline{\text{BACKGROUND}}$ (Output):
This output indicates that the color selected by the RGB outputs is due to background color select rather than a one bit in a display luminance byte. $\overline{\text{BCKGND}}$ may be used to lower the luminance of the background color so that the same color may be used for display of data. This output is blanked (held high) during horizontal and vertical blanking.

GREEN, BLUE, RED (Outputs):
These outputs are used either directly in the TV to generate the selected colors, or indirectly to generate a composite video signal. These outputs are used to indicate the selected color for an "on" spot or the background color for an "off" spot.

$\overline{\text{CSYNC}}$ – $\overline{\text{COMPOSITE SYNC}}$ (Output):
This output is the composite serrated horizontal and vertical sync signal.

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HSYNC – HORIZONTAL SYNC (Output):
This output is a separate horizontal sync signal.

EVS – EXTERNAL VERTICAL SYNC (Input):
A high level at this input sets the line counters to the vertical sync state.

TPB – TIMING PULSE B (Input):
This input is connected to the TPB output of the CDP1802/CDP1804. It is used for strobing the $\overline{MRD}$ and N lines, for horizontal line timing, and as the input to the tone generator.

TPA – TIMING PULSE A (Input):
This input is connected to the TPA output of the CDP1802/CDP1804. It is used for horizontal line timing.

INT – INTERRUPT (Output):
This output is connected to the $\overline{INT}$ input of the CDP1802/CDP1804. One interrupt re-

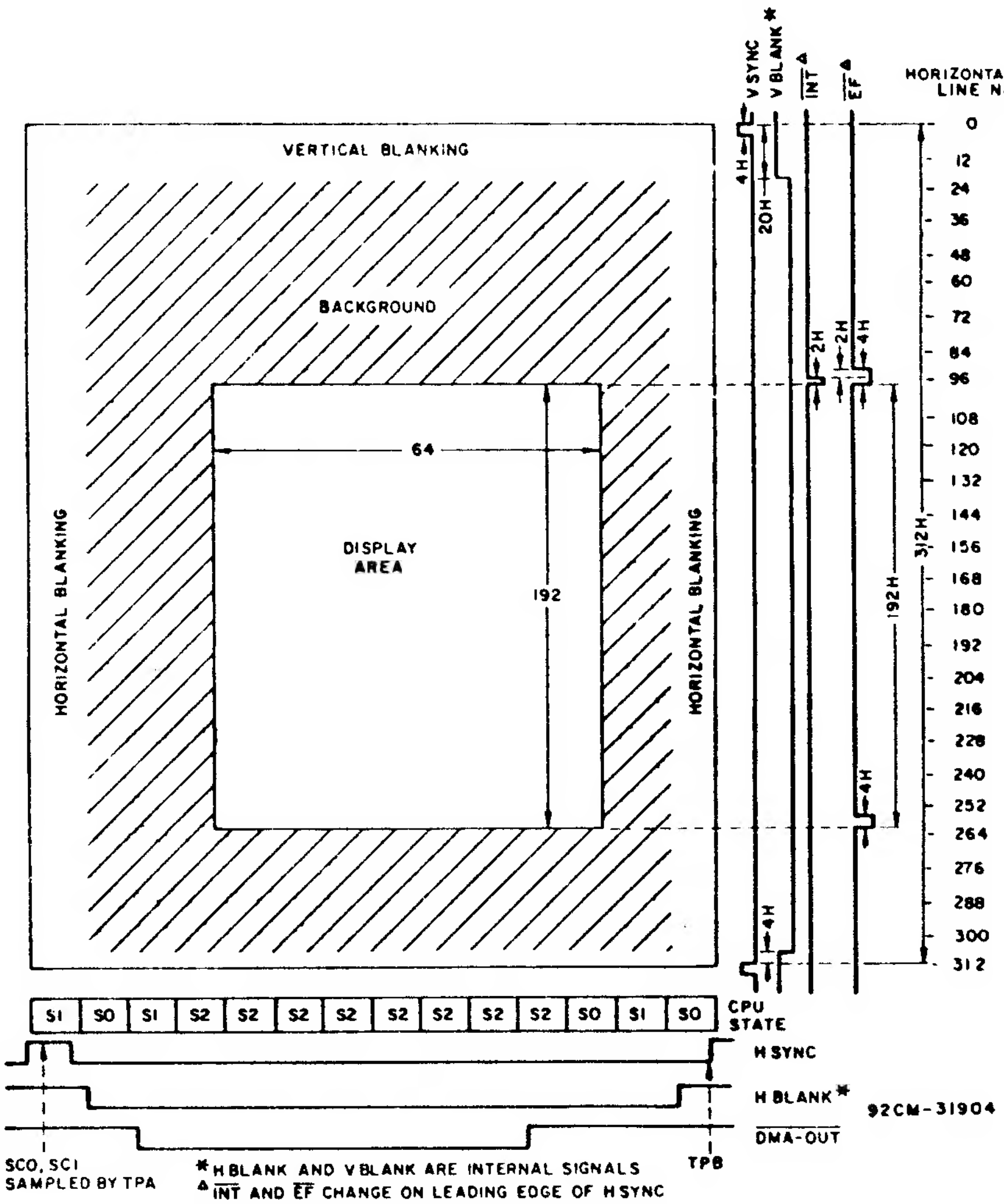

Fig. 4 – Display area diagram.

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quest is issued per field. The request is issued two horizontal lines before the display interval, and the signal remains active for two horizontal lines.

$\overline{\text{DMAO}}$ – $\overline{\text{DMA OUT REQUEST}}$ (Output):
This output is connected to the $\overline{\text{DMAOUT}}$ input of the CDP1802/CDP1804. During the display interval the CDP1864 issues this request for 6 machine cycles during the center of each horizontal line (each line time is 14 machine cycles).

$\overline{\text{CLRIN}}$ – $\overline{\text{CLEAR INPUT}}$:
A low level at this input resets the CDP1864 and generates a low on the $\overline{\text{CLROUT}}$ output.

The requests and the loading of color information are inhibited by reset. These remain inhibited until enabled by the appropriate signals. The line counters and horizontal counters are also held reset while $\overline{\text{CLRIN}}$ is low. The Schmitt trigger circuit at this input allows the use of an RC circuit for power-on reset and reset debounce.

AUD – AUDIO OUT:
This is the output of the programmable frequency generator.

V_{DD}:
Positive supply voltage.

CONTROL LINE TRUTH TABLE

$\overline{\text{MRD}}$	N2	N0	TPB	OP CODE*	OPERATION
X	0	0	X	–	NO ACTION
X	0	1	1	61 or 69	ENABLE REQUESTS
0	0	1	1	61	STEP BACKGROUND COLOR
0	1	0	1	64	LOAD TONE GENERATOR LATCH
1	1	0	1	6C	DISABLE REQUESTS
X	1	1	X	–	ILLEGAL COMMAND
X	X	X	0	–	NO ACTION

* The OP CODE column is given assuming that N1 = 0. It is actually a DON'T CARE because N1 from the microprocessor is not connected to the CDP1864C.

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Machine Code    Assembly Language                Comments

   72           INTRET:  LDXA                    .. RESTORE D
   70                    RET                     .. RETURN
   C4           INT   :  NOP                     .. 3 CYC. INSTR. USED
                                                 .. FOR PGM. SYNC
   22                    DEC R2                  .. R2 IS STACK PTR
   78                    SAV                      . T → STACK
   22                    DEC R2
   52                    STR R2                  .. D → STACK
 F8–B0                   A.1(DISMEM) → RO.1      .. LOAD RO WITH
 F8–A0                   A.0(DISMEM) → RO.0      .. START.ADDR.OF DISP. MEM
 C4, C4                  NOP; NOP                .. NOFS USED FOR SYNC
   E2           DISP  :  SEX2
   80]                   GLO RO                  .. LINE START ADDR. → D
   E2                    SEX2                    .. NOP
   20                    DEC RO                  .. RESET RO.1 IF PASS PG
   A0]                   PLO RO                  .. LINE START ADDR. → RO.0
   E2                    SEX2                    .. NOP
   20                    DEC RO                  .. RESET RO.1 IF PASS PG
   A0]                   PLO RO                  .. LINE START ADDR. → RO.0
   E2                    SEX2                    .. NOP
   20                    DEC RO                  .. RESET RO.1 IF PASS PG
   A0]                   PLO RO                  .. LINE START ADDR. → RO.0
   E2                    SEX2                    .. NOP
   20                    DEC RO                  .. RESET RO.1 IF PASS PG
   A0]                   PLO RO                  .. LINE START ADDR. → RO.0
   E2                    SEX2                    .. NOP
   20                    DEC RO                  .. RESET RO.1 IF PASS PG
   A0                    PLO RO                  .. REPEATS SAME LINE
   3C_                   BN1 DISP                .. LOOPS 32 TIMES
   30_                   BR INTRET               .. END OF DISPLAY
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Fig. 5 – Interrupt routine for a 64 x 32 display.

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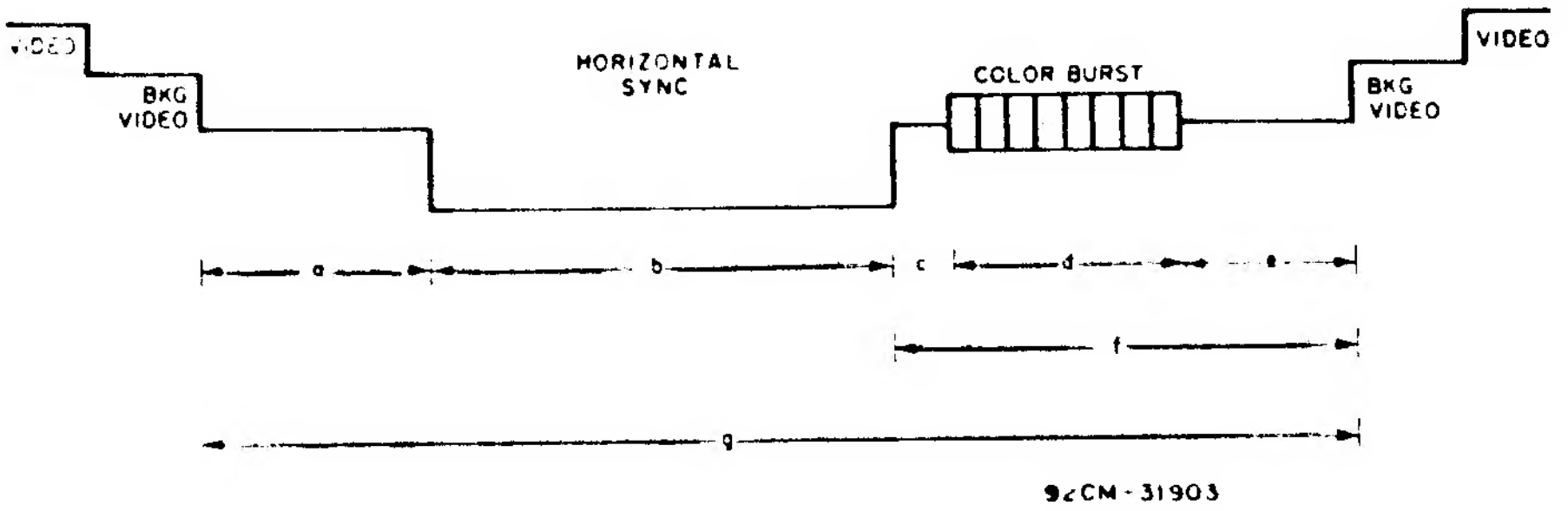
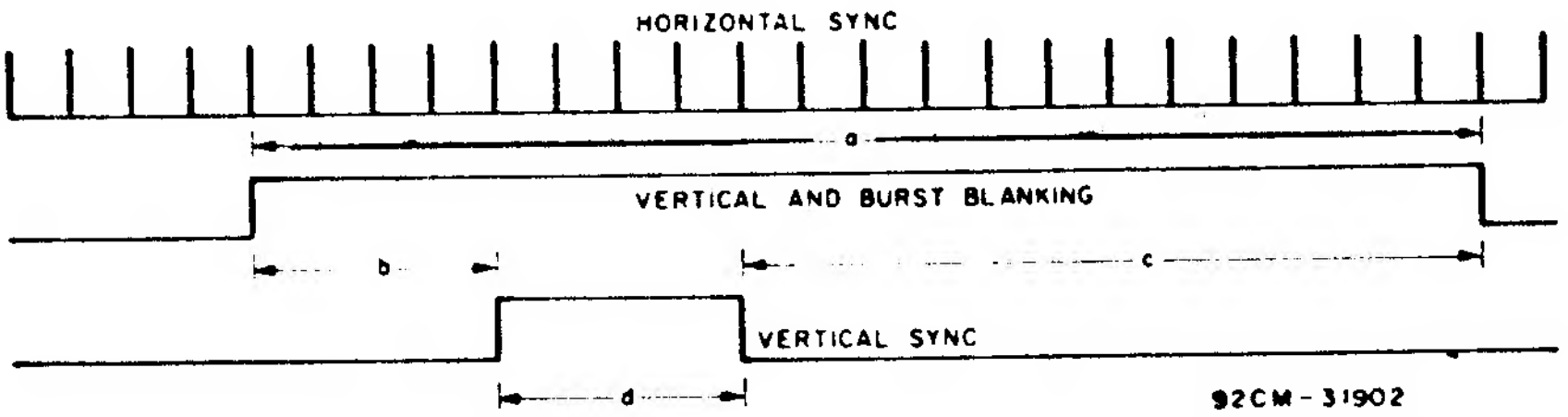


	PAL STANDARD	CDP1864
a	1.55 μs	3.14 μs
b	4.7 ± 0.1 μs	4.57 μs
c	900 ns ± 100 ns	857 ns
d	2.25 ns ± 0.25 μs	2.57 μs
e	2.6 μs	2.0 μs
f	5.8 μs	5.43 μs
g	12.05 μs	13.14 μs
HORZ. FREQ.	15625 Hz	15625 Hz



	PAL STANDARD	CDP1864
a	25 H	24 H
b	2.5 H	4 H
c	20 H	12 H
d	2.5 H	4 H
Burst Blanking	9 H	24 H
Vertical freq. (interlaced)	50 Hz	50
Vertical freq. (non-interlaced)	50 Hz	50.08 Hz

Fig. 6 – Timing diagrams.

CDP1864C Types

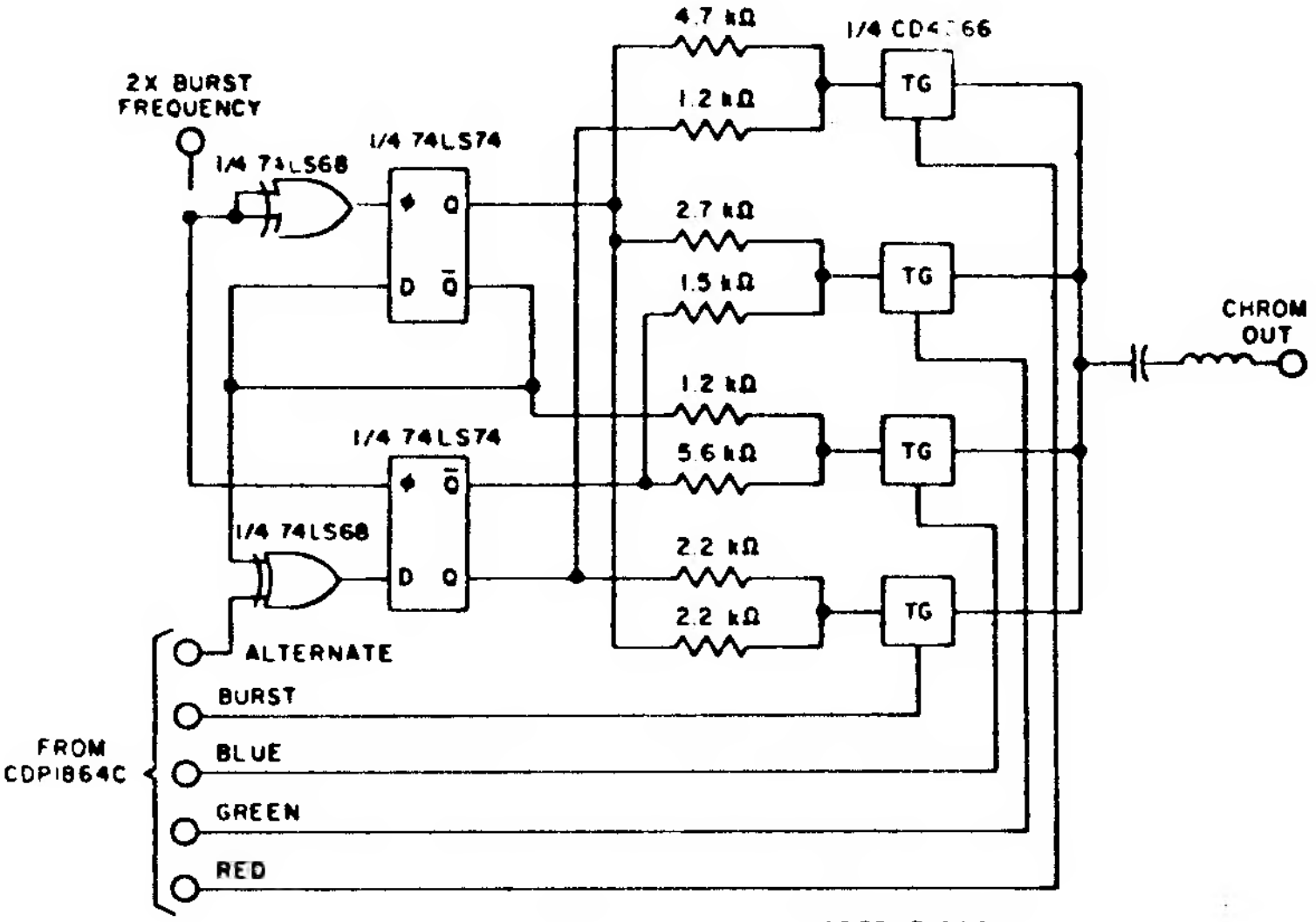


Fig. 7 – Typical color signal generator.

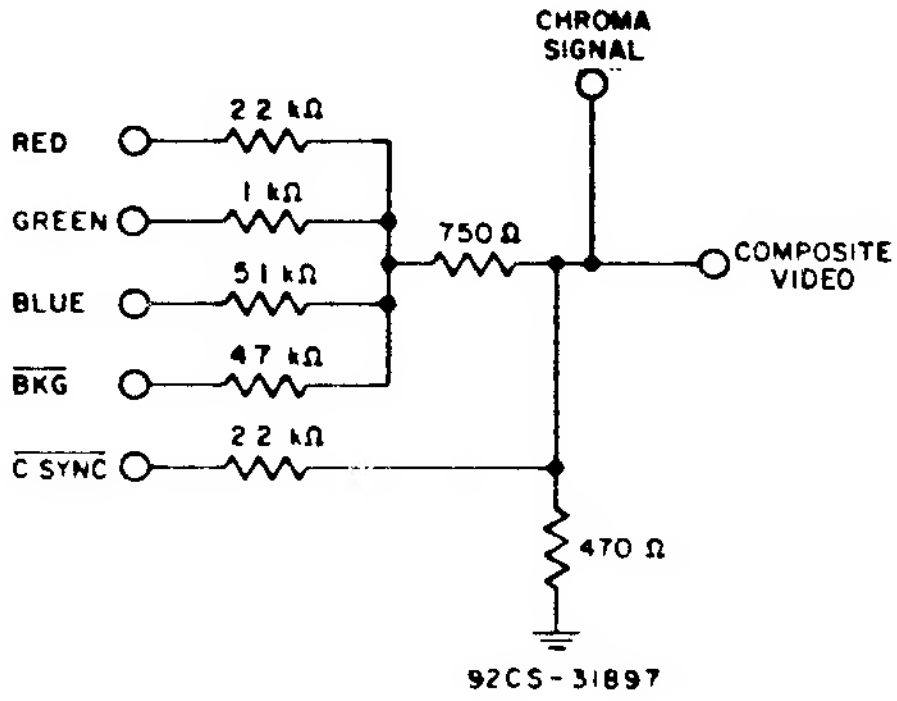


Fig. 8 – Typical composite video network.